AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double brackets indicating deletions.

1. (Currently Amended) An area array type package stack comprising:

at least two packages of area array type disposed to form a stack, each package including

a substrate having a first face and a second face opposing the first face, a plurality of terminal pads and a plurality of connecting pads formed on the second face, and

a semiconductor chip attached to the first face of the substrate and electrically connected to the terminal pads and the connecting pads, the substrate further including a wiring pattern having first wirings connected to the terminal pad and providing electrical paths coupling the semiconductor chip and the terminal pads and second wirings ~~connected~~ connecting [[to]] the terminal pads to the connecting pads to provide ~~and providing~~ electrical paths coupling the ~~semiconductor chip~~ terminal pads and the connecting pads, the first wirings ~~patterns~~ being formed on ~~at least~~ one of the first and the second surface of the substrate, the second wiring being formed on the second surface of the substrate; and

at least one flexible cable having a plurality of conductive patterns thereon extending around at least one side edge of a lower one of the at least two packages, and electrically coupling the connecting pads of the packages through the conductive patterns.

2. (Original) The area array type package stack of claim 1, wherein the semiconductor chip is a center pad type chip.

3. (Original) The area array type package stack of claim 2, wherein the substrate further has first wirings providing electrical paths coupling the semiconductor chip and the terminal pads and second wirings providing electrical paths coupling the semiconductor chip and the connecting pads.

4. (Original) The area array type package stack of claim 1, wherein the semiconductor chip is an edge pad type chip.

5. (Previously Presented) The area array type package stack of claim 4, wherein the second wirings includes vias providing the electrical paths coupling the semiconductor chip and the connecting pads.

6. (Original) The area array type package stack of claim 5, wherein the vias are located in immediate proximity to the connecting pads.

7. (Original) The area array type package stack of claim 1, wherein the connecting pads are arranged in a straight row near an edge of the substrate.

8. (Original) The area array type package stack of claim 1, wherein the connecting pads are arranged in a staggered row near an edge of the substrate.

9. (Original) The area array type package stack of claim 1, further comprising a plurality of external connection terminals formed on the terminal pads of a lowermost package of the packages.

10. (Original) The area array type package stack of claim 1, further comprising a non-conductive adhesive layer interposed between adjacent lower and upper packages.

11. (Original) The area array type package stack of claim 1, wherein each area array type package is a ball grid array package.

12. (Currently Amended) A method for manufacturing an area array type package stack, the method comprising:

providing a first individual package of an area array type (AAT) having a substrate with a first face and a second face opposing the first face, a plurality of terminal pads and a plurality of connecting pads formed on the second face on a flexible cable, wherein the plurality of connecting pads are electrically connected to conductive patterns on the flexible cable, the substrate further including a wiring pattern having first wirings connected to the terminal pads and providing electrical paths coupling ~~a first~~ the semiconductor chip and the terminal pads and second wirings ~~also connected to~~ connecting the terminal pads to the connecting pads ~~and providing~~ to provide electrical paths coupling the ~~first semiconductor chip~~ terminal pads and the connecting pads, the first wirings ~~the wiring pattern~~ being formed on ~~at least~~ one of the first and the second surface of the substrate, the second wiring being formed on the second surface of the substrate;

bending the flexible cable to extend around at least one side edge of the package; and

stacking a second individual AAT package having a substrate with a first face and a second face opposing the first face, a plurality of terminal pads and a plurality of connecting pads formed on the second face on the first AAT package, wherein the plurality of connecting pads are electrically connected to the conductive patterns on the flexible cable, the substrate further including first wirings connected to the terminal pads and providing electrical paths coupling ~~a second~~ the semiconductor chip and the terminal pads and second wirings ~~also connected to~~ connecting the terminal pads to the connecting pads to provide ~~and providing~~ electrical paths coupling the ~~second semiconductor chip~~ terminal pads and the connecting pads.

13. (Original) The method of claim 12, further comprising providing a non-conductive adhesive material between the first and second packages.

14. (Original) The method of claim 12, further comprising forming a plurality of external connection terminals under the first package.

15. (Currently Amended) A method for manufacturing an area array type package stack, the method comprising:

providing a first package of an area array type (AAT) having a substrate with a first face and a second face opposing the first face, a plurality of terminal pads and a plurality of connecting pads formed on the second face on a flexible cable, wherein the plurality of connecting pads are electrically connected to conductive patterns on the flexible cable, the

substrate further including a wiring pattern having first wirings connected to the terminal pads and providing electrical paths coupling ~~a first~~ the semiconductor chip and the terminal pads[[,]] and second wirings ~~also connected to~~ connecting the terminal pad ~~and providing~~ to the connecting pads to provide electrical paths coupling the ~~first semiconductor chip~~ terminal pads and the connecting pads, the ~~wiring pattern~~ first wirings being formed on ~~at least~~ one of the first and the second surface of the substrate, the second wiring being formed on the second surface of the substrate;

forming an adhesive layer under the first package;

attaching a second AAT package having a substrate with a first face and a second face opposing the first face, a plurality of terminal pads and a plurality of connecting pads ~~formed~~ on the second face to the first package by the adhesive layer~~, the substrate further including first wirings connected to the terminal pad and providing electrical paths coupling a second semiconductor chip and the terminal pads, second wirings also connected to the terminal pad and providing electrical paths coupling the second semiconductor chip and the connecting pads~~; and

bending the flexible cable to extend around at least one side edge of the second AAT package wherein the plurality of connecting pads under the second package are electrically connected to the conductive patterns on the flexible cable, the substrate further including first wirings connected to the terminal pads and providing electrical paths coupling the semiconductor chip and the terminal pads and second wirings connecting the terminal pads to the connecting pads to provide electrical paths coupling the terminal pads and the connecting pads.

16. (Original) The area array type package stack of claim 3, wherein the first wirings are formed on the second face of the substrate.

17. (Original) The area array type package stack of claim 5, where the first wirings are arranged on the first face of the substrate and the second wirings are arranged on the second face of the substrate.

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END OF CLAIM LISTING

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